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From:	Andrew C. Graham	Senders Phone No.:	(512) 338-6300

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REGARDING:

Title:	INTEGRATED CIRCUIT INCORPORATING THREE-DIMENSIONAL MEMORY ARRAY WITH DUAL OPPOSING DECODER ARRANGEMENT		
Application No.:	10/774,818	Filed:	February 9, 2004
Examiner:	Unknown	Group Art Unit:	2812
Atty. Docket No.:	023-0025	Confirmation No.:	9232

ATTACHED HERETO:

- (1) Information Disclosure Statement (2 pages)
- (2) Form(s) PTO/1449 (7 pages), with copy of no references;
- (3) Form(s) PTO/SB/08A (1 page), with copy of no references.

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2-23-05

Andrew C. Graham

Respectfully submitted,

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Applicant(s): Mark G. Johnson et al.

Title: INTEGRATED CIRCUIT INCORPORATING THREE-DIMENSIONAL MEMORY ARRAY WITH DUAL OPPOSING DECODER ARRANGEMENT

Application No.: 10/774,818

Filed: February 9, 2004

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INFORMATION DISCLOSURE STATEMENT
37 C.F.R. § 1.97(b)

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- Form(s) PTO/1449 (7 page(s), with copy of no reference(s)).
- Form(s) PTO/SB/08A (1 page(s), with copy of no reference(s)).
- Form(s) PTO/SB/08B (N/A page(s), with copy of no reference(s)).
- Listing of Pending Applications (N/A page(s), with copy of no application(s)).
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Citation of such information shall not be construed as (i) an admission that the information necessarily is, or corresponds to, prior art with respect to the instant invention, (ii) a representation that a search has been made, other than as described herein, or (iii) an admission that the information cited herein is, or is considered to be, material to patentability as defined in § 1.56(b).

For each item of information listed that is not in the English language, the undersigned has provided a concise explanation of the relevance through (i) an English language abstract, (ii) an English language equivalent application, or (iii) if cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action that indicates the degree of relevance found by the foreign office.

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Pursuant to operative regulations, certain copies need not be provided and corresponding information is identified in this Information Disclosure Statement by citation only. In particular,

- In accordance with 37 C.F.R. § 1.98(a)(2)(ii), copies of cited U.S. Patents and U.S. Patent Application Publications are not included.
- Certain information was submitted to, or cited by, the Office in Application No(s). 10/253,354 and 09/939,431, filed September 23, 2002 and August 24, 2001, respectively, to which the above-identified application claims priority under 35 U.S.C. § 120. In accordance with 37 C.F.R. § 1.98(d), copies of that information are not included.
- Pursuant to 1287 OG 163 (October 19, 2004), for those cited pending U.S. patent applications filed (or which entered the national stage under 35 U.S.C. § 371) on or after June 30, 2003 or which are otherwise stored in the USPTO's Image File Wrapper system, copies are not included.

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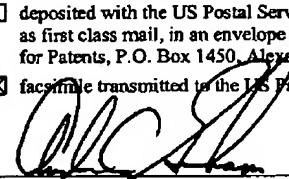
- This Information Disclosure Statement is filed within three months of the filing date of a national application other than a continued prosecution application under § 1.53(d) or within three months of entry of the national stage as set forth in § 1.491 in an international application. Therefore, no fee is required.
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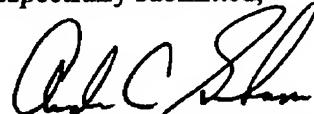
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Date

Andrew C. Graham

Respectfully submitted,



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FORM PTO-1449	SERIAL NO. 10/774,818	ATTY. DOCKET NO. 023-0025
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (use several sheets if necessary)	FILING DATE February 9, 2004	GROUP ART UNIT 2812
APPLICANT(S): JOHNSON ET AL.		

REFERENCE DESIGNATION		U.S. PATENT DOCUMENTS		
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS/ SUBCLASS
A1	3,414,892	12/03/1968	MCCORMACK ET AL.	
A2	3,432,827	03/11/1969	SARNO	
A3	3,576,549	04/27/1971	HESS ET AL.	
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A8	3,787,822	01/22/1974	RIOULT	
A9	3,990,098	11/02/1976	MASTRANGELO	
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A75	5,801,437	09/01/1998	BURNS	
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A78	5,969,380	10/19/1999	SEYYEDY		
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A108	5,960,539	10/99	BURNS		
A109	6,978,258	11/99	MANNING		
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A111	3,863,231	1/75	TAYLOR		
A112	4,229,757	10/80	MOUSSIE		
A113	5,103,422	4/92	TOKITA ET AL.		

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A118	4,442,507	4/10/1984	ROESNER		
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EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS/ SUBCLASS	TRANSLATION YES NO
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A136	JP 60-22352 A	02/04/1985	Japan		Abstract
A137	JP 61222216 A	10/02/1986	Japan		Abstract
A138	JP 63-52483 A	03/05/1988	Japan		Abstract
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A140	EP 0 395 886 A2	11/07/1990	Europe		X
A141	EP 0 516 886 A1	12/09/1992	Europe		X
A142	EP 0 606 653 A1	07/20/1994	Europe		X
A143	WO 94/26083	11/10/1994	WIPO		X

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A144	EP 0 644 548 A2	03/22/1995	Europe		X	
A145	EP 0 516 866 A1	12/09/1992	Europe		X	
A146	WO 98/14763	3/25/1999	WIPO			

EXAMINER INITIAL	OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)
A147	Akasaka, Yoichi, "Three-Dimensional Integrated Circuit: Technology and Application Prospect," Microelectronics Journal, Vol. 20 No. 1 - 2, 1989, pages 105 – 111
A148	Akasaka, Yoichi, "Three-Dimensional IC Trends," Proceedings of the IEEE, Vol. 74, No. 12, December 1986, pages 1703 - 1714
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A151	Frohman-Bentchkowsky, Dov, "A Fully Decoded 2048-Bit Electrically Programmable FAMOS Read-Only Memory," IEEE Journal of Solid-State Circuits, Vol. SC-6, No. 5, October 1971, pages 301- 306
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A154	"3-D Chip-on-Chip Stacking," Industry News, Semiconductor International, December 1991
A155	Inoue, Y., "A Three-Dimensional Static RAM," IEEE Electron Device Letters, Vol. Edl.-7, No. 5, May 1986, pages 327 - 329
A156	Jokerski, N.M., "Manufacturable Multi-Material Integration Compound Semiconductor," SPIE – The International Society for Optical Engineering, Vol. 2524, July 11 – 12, 1995, pages 152 – 163
A157	Kurokawa, Takakazu, "3-D VLSI Technology in Japan and an Example: A Syndrome Decoder for Double Error Correction," Future Generations Computer Systems 4, No. 2, September 1988, pages 145 – 155
A158	Lay, Richard W., "TRW Develops Wireless Multiboard Interconnect System," Electronic Engineering Times, November 5, 1984
A159	Malinik, David, "Memory-Chip Stacks Send Density Skyward," Electronic Design 42, No. 17, August 22, 1994, pages 69 – 75
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A161	Reber, M., et al., "Benefits of Vertically Stacked Integrated Circuits for Sequential Logic," IEEE 1996, pages 121 - 124	
A162	Sakamoto, Koji, "Architecture of Three Dimensional Devices," Bulletin of The Electrotechnical Laboratory, Vol. 51, No. 1, 1987, pages 16 - 29	
A163	Sato, Noriaki, et al., "A New Programmable Cell Utilizing Insulator Breakdown," IEAM Technical Digest, 1985, pages 639 - 642	
A164	Schlaeppli, H.P., "Microsecond Core Memories Using Multiple Coincidence," 1960 International Solid-State Circuits Conference, Digest of Technical Papers, February 11, 1960, pages 54 - 55	
A165	Schlaeppli, H.P., "Microsecond Core Memories Using Multiple Coincidence," IRE Transactions on Electronic Computers, June, 1960, pages 192 - 198	
A166	Stacked Memory Modules, IBM Technical Disclosure Bulletin, May 1995, pages 433 - 434	
A167	Stern, Jon M., "Design and Evaluation of an Epoxy Three-Dimensional Multichip Module," IEEE Transactions on Components, Packaging, and Manufacturing Technology - Part B, Vol. 19, No. 1, February 1996, pages 188 - 194	
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A170	Watanabe, H., "Stacked Capacitor Cells for High-Density Dynamic RAMs," IEDM 1988, pages 600 - 603	
A171	Yamazaki, K., "Fabrication Technologies For Dual 4-KBIT stacked SRAM," IEDM 1986, pages 435 - 438	
A172	"Multilayered Josephson Junction Logic and Memory Devices," Lomatch, S; Rippert, E.D.; Ketterson, J.B., Proceedings of the SPIE-The International Society for Optical Engineering Vol. 2157 p. 332-43	
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A175	"Wide Application of Low-Cost Associative Processing Seen," Electronic Engineering Times, p 43, August 26, 1996	
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FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (use several sheets if necessary)	SERIAL NO. 10/774,818	ATTY. DOCKET NO. 023-0025
	FILING DATE February 9, 2004	GROUP ART UNIT 2812
	APPLICANT(S): JOHNSON ET AL.	

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PTO/SB/08A (Substitute for form 1449/PTO)		Attorney Docket No.: 023-0025				
		Application No.: 10/774,818				
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)		First Named Inventor: Mark G. Johnson				
		Filing Date: February 9, 2004				
		Group Art Unit: 2812				
		Examiner Name: Unknown				
		Date Submitted: February 23, 2005				
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² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04.

³ Enter Office that issued the document, by the two-letter Code (WIPO Standard ST.1).

⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document.

⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible.

⁶ Applicant is to place a check mark here if English language Translation is attached.

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